UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte KOUICHI IKEDA
and
TAKESHI IKEDA

Appeal No. 2005-1230
Application No. 09/716,843

ON BRIEF

Before McQUADE, NASE, and BAHR, Administrative Patent Judges.

NASE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection (mailed June 27, 2003) of claims 5, 6, 8 and 9, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellants' invention relates to a semiconductor device mounted on a memory substrate, a mother board, or the like and a method for manufacturing the same (specification, p. 1). A copy of the claims under appeal is set forth in the appendix to the appellants' brief.

Claims 5, 6, 8 and 9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,786,237[1] to Cockerill et al. (Cockerill).

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejection, we make reference to the answer (mailed August 20, 2004) for the examiner's complete reasoning in support of the rejection, and to the brief (filed May 26, 2004) and reply brief (filed October 19, 2004) for the appellants' arguments thereagainst.[2]

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[1] Issued July 28, 1998.

[2] The rejection of claims 5, 6, 8 and 9 under 35 U.S.C. § 112, second paragraph, set forth in the final rejection was withdrawn by the examiner in the answer.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the patent to Cockerill, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.), cert. denied, 484 U.S. 827 (1987). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it."

The claimed subject matter

Claims 5 and 8, the independent claims under appeal, read as follows:

5. A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor chips on a semiconductor wafer;

a second step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; and

a third step of dividing one of a plurality of pieces of said semiconductor chips on the basis of a result of said quality test,

wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test.

8. A method for manufacturing the semiconductor device, comprising:

a first step of forming a plurality of identical semiconductor chips on a semiconductor wafer;

a second step of carrying out wiring, resin sealing, terminal formation for a plurality of said semiconductor chips formed on said semiconductor wafer;

a third stop of carrying out a quality test of each of a plurality of said semiconductor chips, which is formed on said semiconductor wafer, by using said terminal formed by said second step; and

a fourth step of dividing one or a plurality of said semiconductor chips on the basis of a result of said quality test,

wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible, after said quality test is carried out.

The teaching of Cockerill

Cockerill's invention relates in general to high density electronic packaging which permits optimization of the number of circuit elements to be included in a given volume. Figure 1 is a top view of wafer 11 consisting of multiple integrated circuit (IC) chips 13 which are used in the formation of planar arrays of IC chips. A planar array of IC chips is a single, substantially planar substrate containing multiple IC chips organized in a grid-like (an array) manner. These planar arrays are then used in forming electronic modules.

In accordance with the Cockerill's invention, the wafer is first tested to determine which of the plurality of integrated circuit chips are functional. This step is necessary because some chips may exhibit defects, and their inclusion in the resulting electronic module may be undesirable. In this regard, a "functional map" indicating functional and non-functional chips within the wafer is produced. This map is then utilized, together with information regarding the dimensions of the planar arrays of IC chips required, to produce a "dicing pattern" which indicates how the wafer is to be cut into individual planar arrays of IC chips.

Cockerill teaches (column 3, lines 33-37) that various manual and/or computer controlled methods may be used to determine the dicing pattern. As one particular

process example, if a 1x4 (one chip by four chips) planar array is needed, contiguous linear groups of 4 functional chips are identified. Cockerill further teaches (column 5, lines 28-33) that "other dimensions of arrays of integrated circuit chips are possible (not shown). For example, the array could be two chips wide and four chips long (2x4), or the array could be one chip wide and eight chips long (1x8). Essentially, any combination of array dimensions is possible."

As an enhancement, an optimizing algorithm (i.e., clustering algorithm) may be used in reorganizing the dicing pattern to optimize the total yield of (e.g., 1x4) arrays from the wafer. For example, the algorithm could automatically calculate the preferred orientation of planar arrays on the wafer.

Once a "dicing pattern" is determined, locating each array on the wafer, appropriate transfer metallurgy (i.e. "transfer metals") 15 may be deposited on the wafer using conventional techniques. The transfer metals provide electrical connections from input/output pads (not shown) on the surface of each chip to an edge of the chip. The transfer metallurgy pattern is designed in conjunction with the dicing pattern so that the edges of the chips to which the transfer metals extend corresponds to an edge of the planar array containing the chips. Ultimately, this provides electrical

connectivity from the side surface of a resulting electronic module (defined by the edge surfaces of the individual stacked planar arrays) to individual chips within the module.

The wafer is then diced according to the established dicing pattern along kerfs[3] 17 so as to form planar arrays of IC chips. As a specific example, as shown in Figure 2, an IC chip array 23 has been formed by dicing a wafer 11 into a 1x4 planar array of IC chips 13. Because the array is formed from a single wafer, it comprises a single, substantially planar piece of substrate (for example, silicon) with four IC chips formed thereon. Each IC chip includes transfer metals 15 extending towards an edge surface of the chip (hence, the edge of the array) for connection to external circuitry.

As shown in Figure 3, a plurality of planar arrays of integrated circuit chips are stacked to form electronic module 31 (without side surface metallization). The stacking process may be performed in a manner similar to the forming of "single chip" based electronic modules. Planar arrays of IC chips generally have their active circuit layers protected by an insulator (not shown) that contains appropriate transfer metals. An adhesive (not shown) is applied to the surface of the insulator, and used to adjoin one array of integrated circuit chips to the back surface of the next array. Each array is thus

[3] Kerfs are the spaces between individual chips in a wafer.

bonded to an adjacent array forming a monolithic electronic module. During the stacking process, the arrays are aligned such that the resultant electronic module has a substantially rectangular parallelepiped shape. This results in columnar alignment of IC chips 13 within adjacent arrays of the electronic module. The substantially planar side surface of the module is etched and polished to expose the ends of the transfer metals 15. These transfer metals may be utilized to interconnect the various arrays, and/or connect the module to external circuitry.

Figures 4 and 5 depict embodiments in which side surface metallization 33 has been formed to interconnect the various chips contained in, and facilitate external electrical connection of, the module. As an enhancement, the 1x4 electronic module of Figure 4 may be divided into other variously dimensioned smaller electronic modules. For example, instead of dividing the electronic module into four "chip columns" (1x1) modules, a 1x4 module could be divided into a 1x1 and a 1x3 module. Alternately, it could be divided into two 1x2 modules. Cockerill further teaches (column 5, lines 50-56) that in an alternate embodiment, the size of the individual planar arrays within a module may be different. For example, in a module comprising mostly 1x4 arrays, an end array could be a 1x3 array. As another example, half of a "stack" could comprise 2x8 arrays and the other half 1x8 arrays.

Our decision

We will not sustain the rejection of claims 5, 6, 8 and 9 under 35 U.S.C. § 102(e).

All the claims under appeal recite a particular dividing (dicing) pattern. Cockerill does not disclose the claimed dividing pattern for the reasons set forth by the appellants in the brief and reply brief. The claimed dividing pattern requires the semiconductor chips (which pass the quality check) to be divided into groups of 4 whenever possible, but when groups of 4 are not possible, dividing the semiconductor chips (which pass the quality check) into groups of 2, and when groups of 2 are not possible, dividing the semiconductor chips (which pass the quality check) into groups of 1. Cockerill does not disclose this dividing pattern. Specifically, Cockerill fails to disclose that when a group of four semiconductor chips (which pass the quality check) is not possible that the semiconductor chips (which pass the quality check) are divided first into groups of 2, whenever possible, and then into a group of 1.

For the reasons set forth above, the decision of the examiner to reject claims 5, 6, 8 and 9 under 35 U.S.C. § 102(e) is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 5, 6, 8 and 9 under 35 U.S.C. § 102(e) is reversed.

REVERSED

JOHN P. McQUADE
Administrative Patent Judge

JEFFREY V. NASE
Administrative Patent Judge

JENNIFER D. BAHR
Administrative Patent Judge

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